

Dr. Elizabeth Polgreen

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Education

- 2016 – 2020 **PhD**, *Computer Science*, The University of Oxford.
- 2010 – 2011 **Masters of Engineering**, *Electrical and Electronic Engineering*, The University of Cambridge.
- 2007 – 2010 **Bachelor of Arts**, *Electrical and Electronic Engineering*, The University of Cambridge.

Employment

- 2020 – **Lecturer**, *Laboratory for Foundations of Computer Science*, University of Edinburgh.
My research interests are in program synthesis algorithms, applications of program synthesis and integration of synthesis into verification techniques.
- 2019 – 2020 **Visiting Research Scholar**, *Computer Science*, The University of California, Berkeley.
- Jun 2018 – **Software Development Intern**, *Amazon Web Services*, *Dresden*.
Sep 2018 Applying formal verification techniques to C code for an x86 hypervisor
- Aug 2017 – **Software Development Intern**, *Amazon Web Services*, *Dresden*.
Oct 2017 Development of analysis tools based on formal methods for hot-patching an x86 hypervisor
- Sep 2015 – **Research Assistant in Verification**, *Department of Computer Science*, *University of Oxford*.
Mar 2016 Working with Professor Alessandro Abate on application of machine learning techniques in verification.
- Sep 2013 – **Research Support**, *Department of Computer Science*, *University of Oxford*.
Aug 2015 Lead aspects of research project execution over a broad variety of research projects within the Systems Verification and Validation group.
- Jan 2013 – **Electronics and Software Engineer**, *Peach Innovations*, *Cambridge*.
Aug 2013 Manufacture, testing and debugging of real-time rowing instrumentation systems. Analysis of system output data with view to new product development.
- Aug 2011 – **Electronics and Software Engineer**, *Eg Technology*, *Cambridge*.
Jan 2013 Design engineer developing electronics hardware and software for a variety of consumer and medical devices. Main contributor of C code to embedded software projects using ARM microcontrollers. Further experience in LabVIEW, and contributing to larger team projects written in C#.

Peer-reviewed Publications

- 2023 **Synthesising Programs with Non-trivial Constants**, *authors*, *Journal of Automated Reasoning*, to appear.
- 2022 **UCLID5: Multi-Modal Formal Modeling, Verification, and Synthesis***, *E. Polgreen, K. Cheang, P. Gaddamadugu, A. Godbole, K. Laeuffer, S. Lin, Y. Manerkar, F. Mora, S.A. Seshia*, *Computer Aided Verification (CAV)*, .
- 2022 **Synthesis and Satisfiability Modulo Oracles**, *E. Polgreen, A. Reynolds, S.A. Seshia*, *International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI)*.
- 2021 **The SyGuS Language Standard Version 2.1**, *S. Padhi, E. Polgreen, M. Raghothaman, A. Reynolds, A. Udupa*.

- 2021 **Medley Solver: Online SMT Algorithm Selection**, *N. Pimpalkhare, F. Mora, E. Polgreen, S.A. Seshia*, International Conference on Satisfiability (SAT).
- 2020 **Using model checking tools to triage the severity of security bugs in the Xen hypervisor**, *B. Cook, B. Doebel, D. Kroening, N. Manthey, M. Pohlack, E. Polgreen, M. Tautschnig, P. Wieczorkiewicz*, Formal Methods in Computer-Aided Design (FMCAD).
- 2020 **Automated Formal Synthesis of Digital Controllers for State-Space Physical Plants**, *A. Abate, I. Bessa, D. Cattaruzza, L. Cordeiro, C. David, P. Kesseli, D. Kroening, and E. Polgreen*, Acta Informatica, <https://doi.org/10.1007/s00236-019-00359-1>.
- 2020 **Gradient Descent over Metagrammars for Syntax-Guided Synthesis**, *N. Chan, E. Polgreen, S.A. Seshia*, Workshop of Synthesis (SYNT).
- 2020 **Synthesis in UCLID5**, *F. Mora, K. Chan, E. Polgreen, S.A. Seshia*, Workshop of Synthesis (SYNT).
- 2018 **CounterExample Guided Inductive Synthesis Modulo Theories**, *A. Abate, C. David, P. Kesseli, D. Kroening, E. Polgreen*, Computer Aided Verification (CAV).
- 2017 **Automated Formal Synthesis of Digital Controllers for State-Space Physical Plants**, *A. Abate, I. Bessa, D. Cattaruzza, L. Cordeiro, C. David, P. Kesseli, D. Kroening, and E. Polgreen*, Computer Aided Verification (CAV).
- 2017 **DSSynth: An Automated Digital Controller Synthesis Tool for Physical Plants**, *A. Abate, I. Bessa, D. Cattaruzza, L. Chaves, L. Cordeiro, C. David, P. Kesseli, D. Kroening, and E. Polgreen*, Automated Software Engineering (ASM).
- 2017 **Automated Experiment Design for Efficient Verification of Parametric Markov Decision Processes**, *E. Polgreen, V. Wijesuriya, S. Hasaert, A. Abate*, Quantitative Evaluation of SysTems (QEST).
- 2016 **Data-efficient Bayesian Verification of Parametric Markov Chains**, *E. Polgreen, V. Wijesuriya, S. Haesaert, A. Abate*, Quantitative Evaluation of SysTems (QEST).

Under Submission

- 2023 **mlirSynth: Automatic, Retargetable Program Raising in Multi-Level IR using Program Synthesis**.
- 2023 **Message Chains for Distributed System Verification**.
- 2023 **Towards Building Verifiable CPS using Lingua Franca**.
- 2023 **Reinforcement Learning for Syntax-Guided Synthesis**.

Arxiv

- SynRG: Syntax Guided Synthesis of Invariants with Alternating Quantifiers.**, *E. Polgreen, S.A. Seshia*.
- Verifying Reachability Properties in Markov Chains via Incremental Induction.**, *E. Polgreen, M. Brain, M. Fraenzle, A. Abate*.
- CounterExample Guided Neural Synthesis**, *E. Polgreen, R. Abboud, D. Kroening*.

Invited Talks

- 2022 **Beyond Counterexamples: Synthesis Modulo Oracles**, 11th Workshop on Synthesis.
- 2022 **UCLID5: multi-modal modeling, synthesis and verification**, 3rd Workshop on Democratizing Software Verification.

- 2022 **Model checking Xen**, Verified Software Workshop, Isaac Newton Institute for Mathematical Sciences.
- 2021 **CounterExample Guided Inductive Synthesis Modulo Theories**, The Simons Institute for the Theory of Computing.

Service

Seminar Co-Organiser, *Dagstuhl*, The Future of Reactive Synthesis, September 2023.

Journal Editor, *FMSD*, Special Edition on Synthesis, 2024.

Steering committee, ETAPS, 2022-onwards.

Workshop chair, International Workshop on Synthesis (SYNT), 2021.

Program committees.

2024: TACAS

2023: CAV, SYNT, PriSC, DAV

2022: SMT workshop, SAT, CAV, FMCAD, QEST

2021: CAV (artefact evaluation), TACAS (artefact evaluation), FMCAD, QEST

2019: International Workshop on Synthesis (SYNT)

Non-program committee reviews.

Acta Informatica, Transactions on Programming Languages and Systems, Robotics: Science and Systems 2017, CAV 2021, SOFSEM-FOCS2017, QEST 2017, QEST 2016, Information and Software Technology, 13th International Workshop on Discrete Event Systems

Teaching

2024 **System Design Project**, *University of Edinburgh*, Course Organiser.

2023 **System Design Project**, *University of Edinburgh*, Lecturer.

2022 **Introduction to SAT/SMT**, *Scottish Programming Languages and Verification Summer School*, Lecturer.

2021 **Formal Verification**, *University of Edinburgh*, Course organiser.

2022 **Reasoning and Agents**, *University of Edinburgh*, Tutorials.

2021 **Discrete Maths and Probability**, *University of Edinburgh*, Tutorials.

2020 **Formal Methods: Specification, Verification, and Synthesis**, *UC Berkeley*, Guest Lectures.

2018 **Computer Aided Verification Course**, *University of Oxford*, Guest Lecture.

2020 **Outreach Volunteer**, *Lawrence Hall of Science, UC Berkeley*.

Students

2022-present **Advances and applications of synthesis**, *Yixuan Li*, PhD candidate, University of Edinburgh.

Primary supervisor

2022-present **Verified Lifting**, *José Wesley De Souza Magalhães*, PhD candidate, University of Edinburgh.

Secondary supervisor